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D. Remarks

Rejections of Claims 2 and 20 Under 35 U.S.C. §112, Second Paragraph.

Applicant respectfully requests that this ground for rejection be reconsidered.

The rejection has argued that the term "linearly aligned" is indefinite. Applicant believes this term is not indefinite for a number of reasons set forth below.

First, the terms "linearly" and "aligned" have ordinary and customary meanings. The term "aligned" is understood to be "brought into a line or alignment":

> Main Entry: **align**
> Variant(s): *also* **aline** /ə-'līn/
> Function: *verb*...
> *transitive senses*
> **1** : to bring into line or alignment
> **2** : to array on the side of or against a party or cause...
> (Merriam-Webster Online Dictionary, at http://www.m-w.com).

The term "linearly" is an adverb, and thus modifies "aligned" according to the word "linear":

> Main Entry: **lin·e·ar**
> Function: *adjective*
> **1 a** (1) : of, relating to, resembling, or having a graph that is a line and especially a straight line : STRAIGHT (2) : involving a single dimension **b** (1) : of the first degree with respect to one or more variables (2) : of, relating to, based on, or being linear equations, linear differential equations, linear functions, linear transformations, or linear algebra **c** (1) : characterized by an emphasis on line <*linear* art> (2) : composed of simply drawn lines with little attempt at pictorial representation <*linear* script> **d** : consisting of a straight chain of atoms
> **2** : elongated with nearly parallel sides <*linear* leaf> -- see LEAF illustration
> **3** : having or being a response or output that is directly proportional to the input
> **4** : of, relating to, or based or depending on sequential development <*linear* thinking> <a *linear* narrative>

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lin·e·ar·i·ty /"li-nE-'ar-&-tE/ *noun*

lin·e·ar·ly /'li-nE-&r-lE/ *adverb*

(Merriam-Webster Online Dictionary, at http://www.m-w.com).

Accordingly, the term "linearly aligned" is understood to be "brought into a line or alignment" in a manner "of, relating to, resembling, or having a graph that is a line and especially a straight line, or straight".

For this reason alone, Applicant believes claims 2 and 20 are not indefinite.

The term "linearly aligned" is also understood from the prior art. The prior art is full of this term. As but a few examples, Applicant submits the following uses, which represent but a few of the thousands of examples of the term.

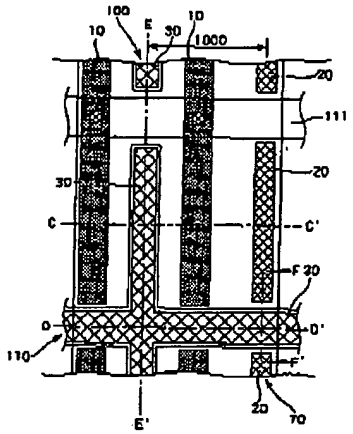
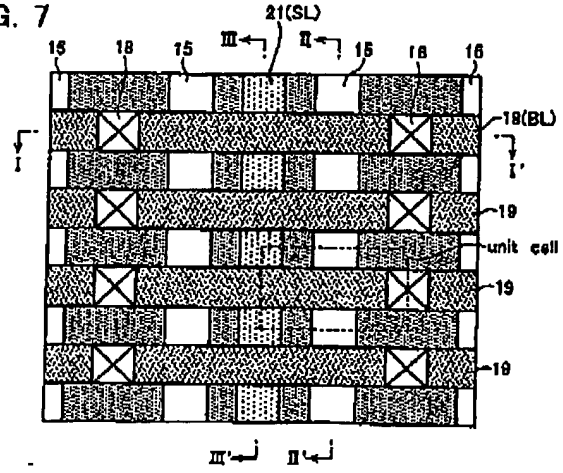


FIG. 17A

The drain layers 70 are ***linearly aligned*** in parallel with the line E-E' under the drain electrodes 20. (U.S. Patent No. 7,067,876, Col. 18, Lines 39-41, emphasis added).

FIG. 7



A bitline 19 is connected through a contact plug 18 to the drain diffusion layer 16b of each of ***linearly aligned*** or "queued" memory cells MC... (U.S. Patent No. 7,027,334, Col. 3, Lines 53-55, emphasis added).

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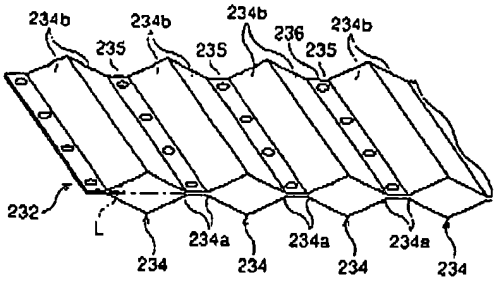
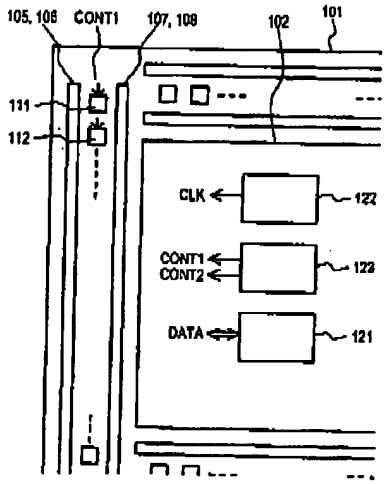
FIG. 7



The longitudinal member 234 are uniformly and ***linearly aligned*** with a longer diagonal line L of the rhomboids, being contiguous with each other. (U.S. Patent No. 6,841,417, Col. 7, Lines 23-25, emphasis added).

The prior art thus illustrates that the term "linearly aligned" is well-understood. Applicant submits the above patents for record and hence for consideration on appeal, not as prior art material to patentability, but as a few of the numerous examples of the use of the term at issue.

Third, this term is illustrated at length in Applicant's Specification:



Also, as shown in FIG. 3, "n" input delay circuits **111** and "n/2" output delay circuits **112**, including a DLL, and the like, can be arranged between the ***linear aligned*** data/signal I/O terminals **(105/106)** and ***linear aligned*** first stage and final stage FFs **(107/108)**. (Applicant's Specification, Page 15, Lines 19-22, emphasis added).

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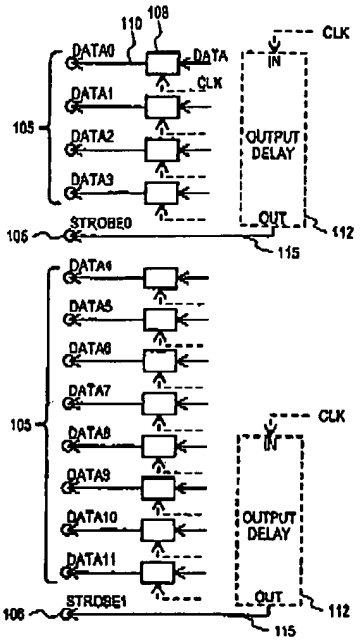

Accordingly, in the case where such output delay circuits **112**, signal I/O terminals **106**, final stage FFs **108**, and output delay circuits 112 (and/or input delay circuits **111**) are ***linear aligned*** as set forth in FIG. 7, the output of delay circuits **112** can be made in close proximity with signal I/O terminals **106**. (Applicant's Specification, Page 24, Lines 18-21, emphasis added).

Accordingly, reference to FIGS. 3 and 7 of Applicant's Specification would show one very particular example of "linear aligned".

Importantly, the above examples should not necessarily be construed as limiting to Applicant's invention. The examples represent but particular embodiments of the invention.

For any or all of the above reasons, Applicant believes that the term "linearly aligned" is not indefinite.

The rejection reasoning argues Applicant's above examples from the Specification remain unclear:

> The Application falls to provide a definition of this term, and it is difficult to comprehend how "m" terminals are **"linearly aligned"** to "n" terminals, especially when "m" is not an integer multiple of "n". (Office Action, dated 04/14/2006, Page 8, Lines 6-9).

Applicant provides an example of such an arrangement below, in the reproduced FIG. 7 from Applicant's Specification:

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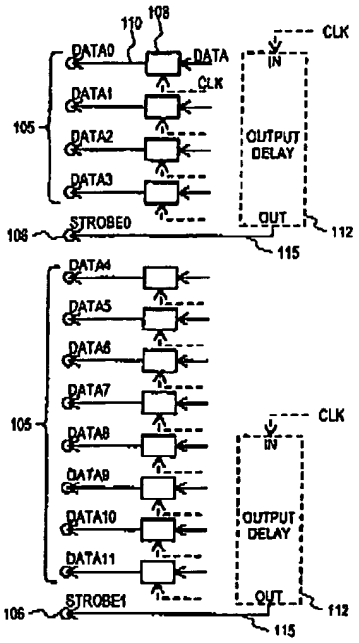
The twelve (e.g., m=12) data output terminals (105) are linearly aligned with the two (e.g., n=2) signal output terminals (106).



Applicant believes that the above illustrates how "m" terminals can be linearly aligned with "n" other terminals.

For all of the above reasons, Applicant requests that this ground for rejection be withdrawn.

Rejection of Claims 1-2, 5 and 7-21 Under 35 U.S.C. §102(e) based on U.S. Patent Publication 2001/0046163 (*Yanagawa*).

The rejection of claims 1-2, 5 and 7-14 will first be addressed.

The invention of claim 1 is directed to a memory controller connected to a semiconductor memory device. The memory controller includes a clock generating circuit, a data generating circuit, "m" data output terminals, and m output holding circuits. The output holding circuits are for storing the output digital data synchronously with the output clock signal. Also included are "n" signal output terminals that provide output strobe signals to the semiconductor memory device in synchronism with the output data, where n < m. A plurality of output delay circuits are included, one output delay circuit for every "p" signal output terminal(s). Each output delay circuit delays the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s). Each output holding circuit is physically

adjacent to a corresponding one of the m data output terminals. Further, the output of each output delay circuit is adjacent to the corresponding p signal output terminal(s)

As is well established, a prima facie showing of anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.[1]

Applicant's claim 1 shows features that believed to be neither shown in nor suggested by the cited reference *Yanagawa*.

1. No "Output delay circuits"

According to Applicant's claim 1, each output delay circuit

1) delays the ***output*** clock signal

2) transmits an ***output strobe*** signal to the corresponding signal output terminal(s), where ***the signal output terminals provide output strobe signals*** to the semiconductor memory device in synchronism with the output data.

To show Applicant's plurality of output delay circuits, the rejection points to various figures and sections of *Yanagawa*:

> As to claim 1, Yanagawa discloses... a plurality of delay circuits... [figure 3 shows a plurality of delay circuits; figures 8-11; figure 15; figure 25; p=1 as a delay circuit is associated with each strobe signal; a data acquisition circuit which delays the strobe signal (abstract); paragraph [0025]... (Office Action, dated 04/14/2006, Page 9, fifth line from bottom to Page 10, line 2).

These figures and sections of the reference cannot show Applicant's output delay circuits as they all are directed to input delay circuits. Applicant has previously illustrated this, at length, without receiving a rebuttal argument.[2] Each cited section of the reference will now be addressed

[1] Scripps Clinic & Research Found. v. Genetech Inc., 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).
[2] See Applicant's Response to Final Office Action.

separately to show that it is directed to an input delay circuit not an output delay circuit, as recited in claim 1.

a. *Yanagawa* "figure 3" does not show any output delay circuits

FIG. 3 of *Yanagawa* shows a data acquisition circuit of FIG. 2:

> FIG. 3 is a block diagram of a first embodiment of the data acquisition circuit 50 according to the present invention. (*Yanagawa*, paragraph [0055]).

However, this data acquisition circuit does essentially the opposite of Applicant's claim language. The data acquisition circuit delays an ***input*** clock signal CLK, not an output clock signal:

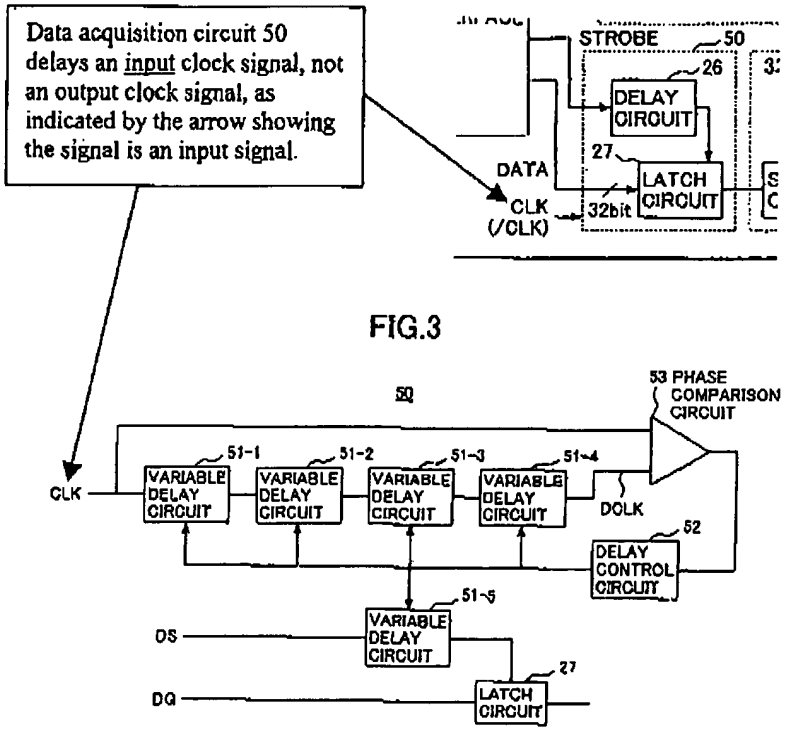


FIG.3

Further, the above shows that an output strobe signal does not "transmit an output strobe signal", where "the signal output terminals provide output strobe signals", as recited in claim 1.

The above is believed to clearly show that FIG. 3 of *Yanagawa* cannot support the

rejection's allegation that an "output delay circuit" of claim 1 is shown by the reference.

b. *Yanagawa* "figure 8-11" does not show any output delay circuits

FIG. 8 of *Yanagawa* shows another example of a data acquisition circuit of FIG. 2.

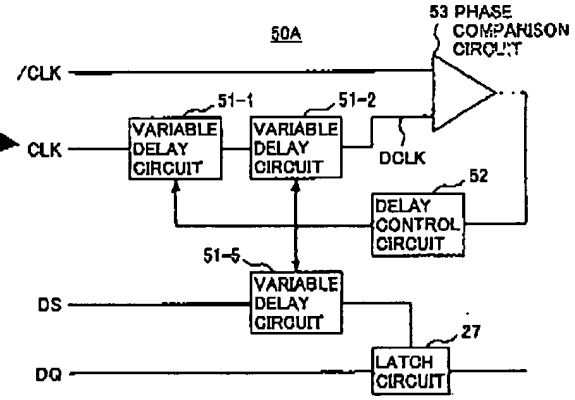
FIG. 8 is a block diagram showing a second embodiment of the data acquisition circuit according to the present invention. (*Yanagawa*, paragraph [0086]).

Clock signal CLK is delayed by variable delay circuits 51-1 and 51-2.

However, as understood from FIG. 2 of *Yanagawa*, this clock is an input clock signal.

No output strobe signal is transmitted from this circuit.

FIG.8

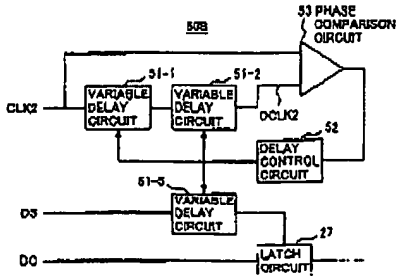


Thus, FIG. 8 of the cited reference shows a circuit that delays an input clock signal, not an output clock signal. Further, the above circuit does not "transmit an output strobe signal".

FIG. 9 of *Yanagawa* shows yet another example of a data acquisition circuit of FIG. 2.

FIG. 9 is a block diagram showing a third embodiment of the data acquisition circuit according to the present invention. (*Yanagawa*, paragraph [0093]).

FIG.9



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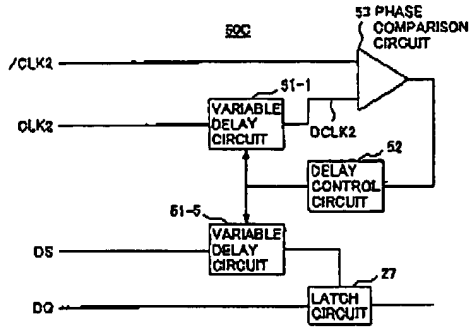
As in the case of FIG. 8, FIG. 9 of the cited reference shows a circuit that delays a double frequency input clock signal CLK2, not an output clock signal, and does not "transmit an output strobe signal".

FIG. 10 of *Yanagawa* shows yet another example of a data acquisition circuit of FIG. 2.

FIG. 10 is a block diagram showing a fourth embodiment of the data acquisition circuit according to the present invention. (*Yanagawa*, paragraph [0099]).

FIG.10

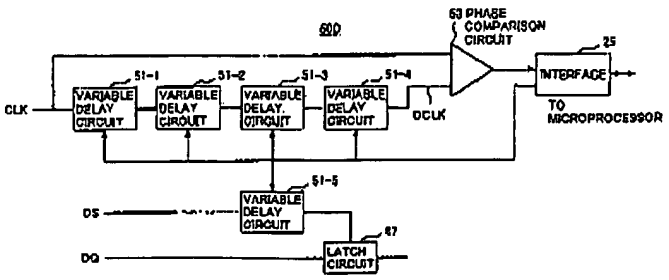


This is no different than FIG. 9. Data acquisition circuit 50C of the cited reference shows a circuit that delays a double frequency input clock signal CLK2, not an output clock signal, and does not "transmit an output strobe signal".

FIG. 11 of *Yanagawa* shows yet another example of a data acquisition circuit of FIG. 2.

FIG. 11 is a block diagram showing a fourth embodiment of the data acquisition circuit according to the present invention. (*Yanagawa*, paragraph [0105]).

FIG.11



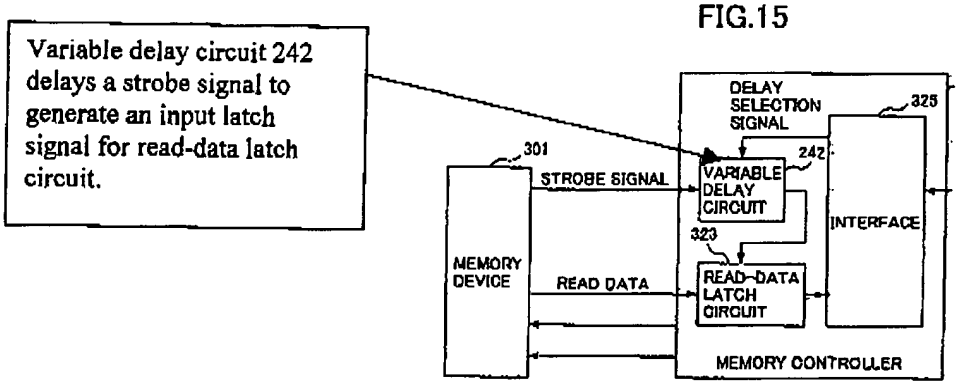
This appears no different than FIG. 3 with respect to Applicant's claim 1. The above circuit delays an input clock signal CLK, not an output clock signal, and does not "transmit an output strobe signal".

For these reasons, cited FIGS. 8-11 of *Yanagawa* cannot show or suggest Applicant's "output delay circuit" as recited in claim 1.

c. ***Yanagawa* "figure 15" does not show any output delay circuits**

With respect to FIG. 15, this figure appears unrelated to "output delay circuits", being directed to the delaying of an input strobe signal (not an output clock signal) to generate an input latch signal (not an output strobe signal):

FIG.15



Accordingly, because the above figures shows neither the delaying of an output clock signal, nor the generation of an output strobe signal, the figure cannot show or suggest Applicant's claim 1 output delay circuit.

d. ***Yanagawa* "figure 25" does not show any output delay circuits**

FIG. 25 of *Yanagawa* shows a variable delay circuit like that of FIG. 16.

> For example, instead of using variable delay circuit of FIG. 16, a variable delay circuit as shown in FIG. 25... may be employed. (*Yanagawa*, paragraph [0145]).

However, FIG. 16 is unrelated to delaying of output clock signals to transmit output strobe

signals. Instead, FIG. 16, like FIG. 15 of *Yanagawa*, teaches the delaying of a strobe signal, not an output clock signal:

> FIG. 16 is a circuit diagram showing the configuration of the variable delay circuit 242. The variable delay circuit delays a signal IN(strobe signal)... (*Yanagawa*, paragraph [0133]).

Accordingly, FIG. 25 cannot show Applicant's output delay circuit, either.

e. ***Yanagawa* ABSTRACT does not show any output delay circuits**

The Abstract of *Yanagawa* recites the following:

> [A] data acquisition circuit which delays the strobe signal...

This statement, of course, refers to the various data acquisition circuits discussed at length above. As such, it cannot show Applicant's claim 1 limitations as such circuits delay input strobe signals, or input clock signals, rather than an output clock signal. Further, none of the data acquisition circuits transmits an output strobe signal, where signal output terminals provide such output strobe signals to the semiconductor memory device.

f. ***Yanagawa* paragraph [0025] does not show any output delay circuits**

Paragraph [0025] of *Yanagawa* is the brief description of FIG. 8. As noted above, FIG. 8 cannot show or suggest Applicant's "output delay circuits".

2. No "Plurality of output delay circuits" that each "transmit an output strobe signal"

All embodiments of *Yanagawa* show a single output strobe signal. Accordingly, the reference cannot anticipate Applicant's claim 1.

Applicant will review all figures of the reference to illustrate this fact.

FIGS. 1 and 2 of *Yanagawa* shows one output strobe signal, shown as STROBE SIGNAL going from memory controller 10 to memory device 11.

FIG. 3 and 8-11 do not show any output strobe signal, but rather an input strobe signal

DS.

FIG. 4 shows a delayed input clock signal as OUTPUT OF VARIABLE DELAY CIRCUIT 51-1.

FIG. 5 shows delay control and phase comparison circuits for input clock signals CLK and /CLK.

FIGS. 6, 7, 16, 17A, 17B, 18 and 25 show variable delay circuits that can delay an input clock signal CLK, input strobe signal, or input data signal DQ, but never described as delaying an output strobe signal.

FIGS. 12, 13A, 13B, 15 show a single input strobe signal STROBE SIGNAL, not an output strobe signal.

FIG. 14 shows a single input strobe signal (input to 241), not any output strobe signal.

FIG. 19 shows a procedure for setting a delay. The procedure provides no teachings related to an output strobe signal.

FIGS. 20A and 20B show operations for checking a read timing and make no reference to any output strobe signals.

FIGS. 21-24 show timing operations during adjustment processes and make no reference to any output strobe signals.

Accordingly, *Yanagawa* does not show or suggest a plurality of output delay circuits, as recited in claim 1.

3. No "m holding circuits wherein each m output holding circuit is physically adjacent to a corresponding one of the m data output terminals".

Applicant does not believe that rejection can show the above limitation is shown or suggested by *Yanagawa*.

In rejecting claim 1, the rejection relies on the following reasoning:

> Yanagawa discloses... **"m" data output terminals**.... [figure 2, 32 bits DATA to and from the memory device, m=32]... **m output holding circuits**... [32 bits latch circuits (figure 2, 30, 31 and 27)]... **wherein each m output holding circuit is physically adjacent to a corresponding one of the m data output terminals** [figures 2, 5-7; refer to "Response to remark on claim 1"] (See the

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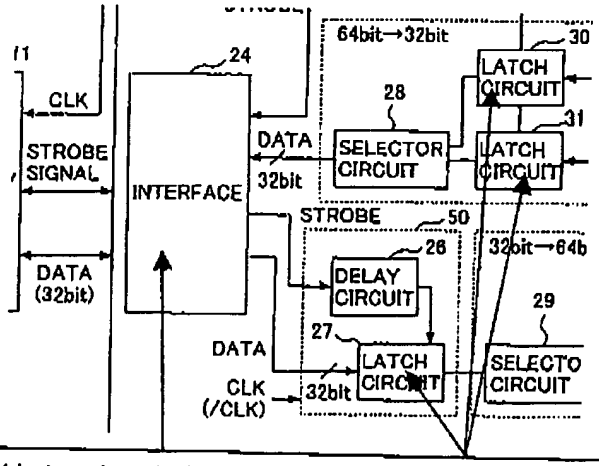
> Office Action, dated 04/14/2006, Page 9, 5th line from bottom to Page 10, Line 19).

Thus, the rejection reasoning argues that 32-bit latches 30, 31 and 27 are "physically adjacent" to a bus DATA(32 bit).

However, the same rejection then takes a contradictory position when addressing Applicants' previous response:

> [T]he only entity between the 32-bit DATA connection port and the 32-bit DATA output signals is an INTERFACE unit (figure 2, 24). (Office Action, dated 04/14/2006, Lines 14-15).

The fact that there is an interface unit between any output terminals of memory controller 10 in *Yanagawa* and the 32 bit latch circuits (30, 31, and 27), alleged to correspond to applicant's m output holding circuits, is inconsistent with "each m output holding circuit being physically adjacent to a corresponding one of the m data output terminals" as recited in claim 1:



If interface 24 is the only entity between bus DATA(32 bits) and the 32-bit connection port, then latch circuits 30, 31 and 27 cannot be physically adjacent to bus DATA(32 bits).

Conversely, if latch circuits 30, 31 and 27 are physically adjacent to bus DATA(32 bits), interface cannot be the only entity between bus DATA(32 bits) and the 32-bit connection port.

Accordingly, because the rejection relies on an inconsistent interpretation of the reference, Applicant believes a prima facie case of anticipation cannot have been established, and this ground for rejection is traversed for this additional reason.

Various claims depending from claim 1 are believed to be separately patentable. Claim 2, which depends from claim 1, recites a number of limitations, including

1) output holding circuits linearly aligned with one another;

2) signal output terminals linearly aligned with output data terminals;

3) output delay circuits linearly aligned with one another between the holding circuits and the aligned data output terminals/signal output terminals.

Yanagawa discloses a memory controller with a data latch operation. However, the reference is entirely silent as to the alignment of any circuit features, let alone the very particular features recited in claim 1.

To show the above emphasized claim limitations, the rejection points to FIG. 2 of *Yanagawa*, and argues certain features are "consistent" with certain of Applicant's figures:

> As to claim 2, Yanagawa teaches that the m output data terminals and n signal output terminals are linearly aligned with one another [figure 2 shows that the 32-bit DATA terminals are physically located at the left-had side of the INTERFACE unit and the 32-DATA output signals are physically located at the right-hand side of the INTERFACE unit, and there is one-to-one correspondence between the two groups of 32-bit DATA signals. Note that this is consistent with the illustrations of figures 3 and 7 of the Application] (Office Action, dated 04/14/2006, Page 11, Lines 1-7).

Applicant notes that FIG. 2 of *Yanagawa* shows 32-bit data, however, this figure shows no alignment of any of the above emphasized claim features:

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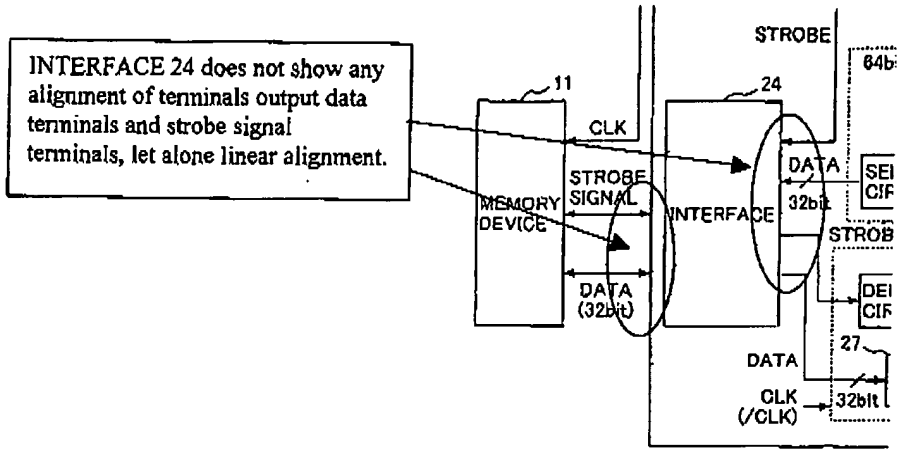

Applicant notes that the text provides no inherent teaching of such a feature, either. A review of the discussion of FIG. 2 in *Yanagawa* (see paragraphs [0048] to [0054] of the reference) provides no mention of any terminals, or alignment of any features.

In addition or alternatively, the rejection is inconsistent in applying the reference. The rejection reasoning related to Applicant's "holding circuits" is as follows:

> [T]he m holding circuits are linearly aligned with one another [***figure 25***; Note that this is consistent with figures 3 and 7 of the Application]... (Office Action, dated 04/14/2006, Page 11, Lines 7-9, emphasis added).

Thus, the rejection relies on FIG. 25 of *Yanagawa* to show linearly aligned holding circuits. However, this same figure was utilized to show "output delay circuits", an entirely different element in rejecting claim 1.

> As to claim 1, Yanagawa discloses... a plurality of delay circuits... [figure 3 shows a plurality of delay circuits; figures 8-11; figure 15; ***figure 25***... (Office Action, dated 04/14/2006, Page 9, fifth line from bottom to Page 10, line 2, emphasis added).

Thus, if FIG. 25 shows linearly aligned holding circuits, this same figure cannot also show delay circuits.

Because the rejection of claim 2 is inconsistent with that of claim 1, the rejection is believed to be improper and should be withdrawn.

Claims 8 and 14, which depend from claim 1, are believed to be separately patentable over the cited reference.

Claim 8 recites "a first wiring corresponding to each data input terminal that transmits digital data to a corresponding input holding circuit, and a second wiring corresponding to each input holding circuit that transmits the input strobe signal from a corresponding input delay circuit to the input holding circuit. The first and second wiring corresponding to each input holding circuit being essentially equal in length".

Claim 14 recites "m input holding circuits... each input holding circuit comprising a second latch circuit connected to a corresponding data I/O terminal by a first wiring... an input delay circuit connected to each signal I/O terminal by a second wiring, each input delay circuit delaying a received device input clock from the semiconductor memory device signal by a predetermined amount to generate an input strobe signal, each input strobe signal being connected to a corresponding second latch circuit by a third wiring; wherein the length of the first wiring to each second latch circuit is essentially equal to the sum of the lengths of the second and third wirings corresponding to the same second latch circuit.

Yanagawa provides not teachings related to wiring, let alone wiring lengths. A word search of *Yanagawa* for the term wir$ (where $ is a wildcard) provides no matches. The rationale relied upon to reject claim 8, is unrelated to wiring as well:

> Yanagawa teaches that "even when the delay of the variable delay circuits varies due to a variety of variation factors such as variation of the manufacturing process, variation in ambient temperature, and variation in the power supply voltage, proper delay control based on the phase comparison of clock signals makes it possible to adjust the delay of the variable delay circuit 51-5 to be equal to the 1/4 cycle of the clock signal. Under the conditions in which a variety of variation factors are present, therefore, optimum data acquisition timing can be achieved" (paragraph 0064).
>
> Since it is possible to adjust the delay of the variable delay circuits to be equal to the ¼ cycle of the clock signal, the wirings, or signal paths, are

essentially equal electrically for the purposes of signal synchronization. (Office Action, dated 04/14/2006, Page 6, Lines 1-10)

The above reasoning cannot have presented a prima facie case of "essentially equal wiring lengths" as it never indicates anything about wiring lengths. The reasoning has provided no citation or other explanation of how delays using variable delay circuits shows wiring lengths as recited in claims 8 and 14.

The rejection of claims 15-21 will now be addressed.

The memory controller of claim 15 includes a predetermined number "m" data input terminals, a predetermined "n" signal input terminals, a data storing circuit, n input delay circuits, m input holding circuits, m signal input wirings and m signal input wirings. The predetermined number "m" data input terminals receive input data from the semiconductor memory device. Each signal input terminal receiving a device input clock signal from the semiconductor memory device in synchronism with the input data, where m > n. The data storing circuit receives digital data from the data input terminals. The n input delay circuits delay received device input clock signals from the semiconductor memory device by a predetermined amount to generate input strobe signals. The m input holding circuits hold the input data in synchronism with the input strobe signals generated by the input delay circuits. Each data input wiring transmits an input data value from one data input terminal to a corresponding input holding circuit. The m signal input wirings transmit one input strobe signal from one input delay circuit to a corresponding input holding circuit. The data input wiring and signal input wiring for the same corresponding input holding circuit being essentially equal in length.

The cited reference *Yanagawa* discloses a memory controller that provides an interface between a microprocessor having a 64-bit data width and a memory device that has a 32-bit data width. The controller includes latch circuits (27), argued to correspond to Applicant's m input holding circuits[3] that latch a 32-bit data supplied from the memory device.[4]

[3] See Page 3, lines 11-12 of Office Action dated October 12, 2005.
[4] See FIG. 2 in conjunction with paragraph [53] of *Yanagawa*.

However, Applicant does not believe that *Yanagawa* shows a data input wiring and signal input wiring for the same corresponding holding circuit being "essentially equal in length" as recited in claim 15.

To address this ground for rejection, Applicant incorporates by reference herein the comments set forth above for claims 8 and 14 are incorporated by reference herein.

Accordingly, because *Yanagawa* does not show all elements of claim 15, this ground of rejection is traversed.

Claim 20 is believed to be separately patentable over the cited reference.

Claim 20, which depends from claim 15, recites that the m data input terminals and n signal input terminals are linearly aligned with one another; and the m input holding circuits are linearly aligned with one another parallel to the data input terminals and signal input terminals.

To address this ground for rejection, Applicant incorporates by reference the comments set forth above for claim 2.

Rejection of Claims 3, 4, and 6 Under 35 U.S.C. §103(a), based on *Yanagawa* in view of US Patent Publication 2001/0014922 A1 (*Kuge*).

As is well known, in proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a prima facie case of obviousness based on the prior art.[5]

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[6]

To the extent that this ground for rejection relies on *Yanagawa*, the arguments set forth above with respect to claim 1 are incorporated herein by reference. Namely, *Yanagawa* does not show or suggest all the limitations of an "output delay circuit" nor "a plurality of output delay circuits". Though not relied upon by the rejection to show such limitations, *Kuge* also does not teach such a limitation element.

For this reason this ground for rejection is traversed.

[5] Ex parte Obukowicz, 27 USPQ 1063, 105 (B.P.A.I. 1992).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

The present claims 1-21 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314

[6] MPEP §2143.